Final Exam Information

The exam will be comprehensive. The following topics will be included:

- Basic concepts of computer organization—datapath, registers, assembly language, instruction sets, etc. (P&H chapter 1)
- Basic notions of computer performance (P&H chapter 1)
- Programming in C (K&R chapters 1–5, selected sections; appendices on specific library functions such as `printf`, `getchar`, etc.)
- Instruction sets: MIPS (P&H chapter 2)
- Arithmetic, binary, twos-complement, floating point (P&H chapters 2, 3)
- Digital logic, circuits, simple datapath (P&H chapter 4, appendix C)
- Memory (P&H chapter 5)

1. For examples of problems dealing with the basic performance equation, see any of exercises 1.3, 1.4, 1.5 in P&H, as well as the examples in the chapter. Most of these are probably more elaborate than what I could ask on an exam, and some involve defining new concepts, e.g., “peak performance,” which I would not do on an exam. The basic performance equation is the key concept here, for instance, given a clock speed, cycles per instruction for various types of instruction, number of instructions of each type, find the execution time.

2. What is the difference, if any, between the MIPS branch instruction, `b`, and the MIPS jump instruction, `j`?

3. What does the following C program segment print out?

```c
... int i = 15, j = 20;
int *m = &i;
int *n = &j;
i = 50;
*n = 40;
*m = *m + 1;
printf("i = %d, j = %d, *m = %d, *n = %d\n", i, j, *m, *n);
...```

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4. A certain signed 32-bit integer (in twos-complement representation) has the hexadecimal value 0xFFFFF0A8. What is the signed decimal value of this integer?

5. Using AND, OR, and NOT gates only, construct a circuit that realizes the following three-input boolean function:

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<th>A</th>
<th>B</th>
<th>C</th>
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6. What is the difference between a write-through and a write-back scheme (with reference to memory hierarchies)?

7. What is the difference between direct-mapped and associative caching schemes?

8. What is the difference between a compiler and an assembler?

9. Using only AND, OR, and NOT gates, design a logic circuit for a multiplexer that takes two input bits $A$ and $B$ and a control bit $C$. When $C = 0$, the output of the multiplexer is the value of $A$; when $C = 1$, the output of the multiplexer is the value of $B$.

10. What do the authors name the two components of the CPU?

11. A memory cache consists of 8 blocks, each containing 4 32-bit words. Assuming that a direct-mapped caching method is used, and assuming that the cache is initially empty, which blocks in the cache are marked as “valid” after the following sequence of memory references (we assume a byte-addressed memory, so all of the references are given as multiples of 4)? Which memory references are hits and which ones are misses?

$$0, 16, 64, 8, 128, 0, 20$$

12. How many distinct bytes of memory (in gigabytes) can be referenced using a 32-bit address, assuming a byte-addressable memory (i.e., each byte has a distinct address)?

13. In a 4-way set-associative cache using 2-word block sizes, how many sets are there in a 1024-word cache?

14. In C, what does the following code segment produce?

```c
...  
int i = 50;  
int j = i>>1;
```
j = i & j;
printf("j = %d\\n", j);
...

15. Explain the steps in a basic instruction cycle in a MIPS processor; assume the instruction
requires a memory access. Include a description of what happens to the $pc$ register. You
may refer to the figure below.